Design of Single Carrie-Frequency Domain Equalization System Based on FPGA

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Abstract: With the development of communication technology, putting forward higher requirements for the city's communication rate. Due to the complex environment in the city, there is a serious multipath fading effect in the communication process of broadband wireless channel transmission, which has a great negative impact on the transmission of information and greatly improves the bit error rate. In order to overcome the degradation of communication quality caused by multipath effects, communication technology workers have proposed kinds of techniques anti-multipath effects, which also help single carrier frequency domain equalization (SC-FDE) overcomes the effectiveness of multipath fading in digital communications. Therefore SC-FGE has been widely used. This paper introduces the mainstream technology against multipath effect based on the principle of multipath effect, then analyze the design of single carrier frequency domain equalization system in detail, and implements the system on FPGA platform to test the final bit error rate and other indicators.

1. The principle of multipath fading channel and the main technical means

In the process of electromagnetic wave propagation in mobile communication, the modes of propagation mainly include direct radiation, scattering and reflection. If only analyze one direct wave and one reflected waved, when the path of the reflected wave changes will cause the path difference changed, which making the phase of the two signals received at the receiving point change. At present, the working environment of communication mobile stations is often in urban buildings. Such communication environments have the characteristics of complex terrain and diverse electromagnetic wave propagation modes. Due to the mobile station antenna basically lower the height of the urban building, it is difficult to transmit directly. Therefore, the wave propagation between the base station and the mobile station tends to have reflected signal of multiple paths, and the signal received by the receiving end is synthesis result of waves from different propagation paths.

Due to the difference in propagation path and reflector properties, each wave at the receiving point has a random amplitude and phase. In the same communication environment, multiple reflected waves will form standing wave effect, so that the received signal energy at the receiving end changes significantly with time. Different bands and modes of propagation have dofferent principle of multipath propagation, which also causes the complexity of analyzing multipath effects. Multipath effects will have a large negative impact on digital communications in cities.

The figure below is a schematic diagram of the formation of multipath effects.

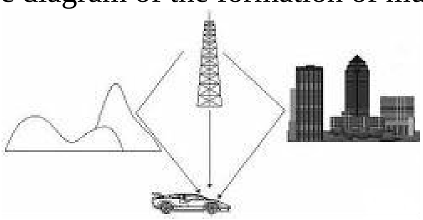

Fig.1 Schematic Diagram of the Formation of Multipath Effects

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The densely populated building in the city formed multipath effect, and caused the channel fading is serious, and the channel is time-varying. From the perspective of short-range communication, the signal envelope satisfies the Rayleigh distribution and satisfies the standard normal distribution. The delay spread caused by multipath effect makes Inter Symbol Interference (ISI) serious, which makes the reliability of communication quality not guaranteed. Therefore, some technical means are urgently needed to reduce the impact of multipath effects. At present, the main anti-multipath effect technologies in the communication industry include multipath diversity receiving technology, frequency hopping technology, direct spread spectrum technology, single carrier time domain and frequency domain equalization technology.

The basic idea of multipath reception is that the fading of an incoherent signal is also irrelevant. By acquiring two or more irrelevant signal samples, the probability that these signals are simultaneously below a given level is much lower than the independent signal. It can be seen that a suitable composite signal of different values can have a smaller multipath fading than a single signal.

The basic idea of diversity reception is to separate the received multipath signals into incoherent or independent multiplex signals, and then combine the energy of these multiplex signals according to certain rules to maximize the received useful signal energy. Improve the signal-to-noise power ratio at the receiving end, and minimize the bit error rate for digital systems.

The concept of multipath diversity is based on the time delay spread of multipath signals. If the received multipath signals can be separated, it is possible to try to only receive the signals of the main path or combine the separated multipath signals to increase the energy of the useful signals. This is the separation and merging of multipath signals, with the aim of reducing inter symbol interference caused by delay spread. However, the multipath signal received usually has a small delay difference, and it is random. The superimposed multipath signal is generally difficult to separate, only a specific designed signal can be separated. This signal named spread spectrum signal.

The principle of frequency hopping anti-multipath is that if the carrier frequency of the transmitted signal is f, when there is a multipath propagation environment, the time of signals arrive at the receiving end depends on different transmission delays of different paths. The receiver can achieve the effect of reducing the multipath effect by performing carrier frequency conversion. At present, there is still a technical difficulty in implementing a frequency hopping communication system with high frequency hopping. Therefore, the current use of frequency hopping technology in digital mobile communications is mainly anti-interference and anti-fading. In the TDMA system, in order to improve the transmission performance of digital communication and increase the system capacity, that is, to reduce the effects of deep fading and co-channel interference, slow frequency hopping technology is necessary.

2. Introduce of FPGA hardware platform

FPGAs are field-programmable gate arrays that have evolved from programmable devices such as PLDs. Due to the shortcomings of high cost of production and high cost of application-specific integrated circuits (ASICs), FPGAs have entered the historical arena as a semi-custom circuit.

FPGA adopts the concept of logic cell array LCA. FPAG is composed of CLB and IOB. At present, there are many kinds of FPGAs, such as XC series of XILINX, TPC series of TI company, FIEX series of ALTERA company, etc.

First, FPGA design ASIC circuit solves the problem that ASIC circuit needs to be customized. Although the performance is somewhat reduced, it saves a lot of time and economic cost.

Second, FPGA is rich in internal resources, it can realize a large number of logic circuit combinations, and has a wealth of input and output pins, which is convenient for joint development with external chips.

Third, In the ASIC circuit, the design FPGA has a short cycle, low cost, and low risk.

Forth, compared with the single-chip circuit, the operation of the single-chip microcomputer is based on ARM and other architectures, and the FPGA chip can execute multiple instructions in parallel, which greatly improves the running speed, processing capacity and system processing capacity of the chip.

Due to the above advantages of the FPGA chip, it has become a chip development method favored by developers in the field of hardware circuit design. With the development of information science, the throughput and processing speed of the system are getting higher and higher. With the development of information science, higher requirements have been put forward for the throughput and processing speed of the system, even by continuously reducing the minimum MOS tube size of the chip device and optimizing the pipeline design, the original sequential execution mode is more and more difficult to meet the processing real-time. The parallel processing capability of FPGA has made it widely used in the fields of communication, image processing and artificial intelligence.

3. Overview of single carrier frequency domain equalization technology

Channel equalization refers to Use the equalizer at the receiving end to compensate for the channel characteristics by studying the frequency domain or time domain transmission characteristics of the signal, so that the "transmission channel" has better transmission characteristics including the equalizer, which is used to cancel Inter-symbol interference caused by multipath channel. Equalization can be divided into frequency domain equalization and time domain equalization. Frequency domain equalization adjusts the transmission function in the frequency domain angle, corrects amplitude characteristics and group delay characteristics, so that the channel satisfies the distortionless transmission condition. In digital communications, time domain equalization techniques are often used. The technique of eliminating the influence of multipath effects by using the impulse response satisfies the condition of no intersymbol interference.

The OFDM system achieves equalization in the frequency domain. Its implementation principle is: at the transmitting end, the IFFT technology is used to perform data modulation on orthogonal subcarriers, thereby eliminating channel weakness. OFDM has high spectrum utilization and low system complexity, but the effect of OFDM is greatly affected by the carrier synchronization effect, and the requirements for the RF front end are high. Single-Carrier Frequency Domain Equalization (SC-FDE) is an effective technique for overcoming multipath fading in broadband wireless transmission digital communication. It combines the advantages of OFDM technology and single-carrier transmission, and corresponds to time-domain equalization. The frequency characteristics compensate for the amplitude-frequency characteristics of the actual channel and the distortion of the phase-frequency characteristics. Compared with the previous transmission technology, single-carrier frequency domain equalization has the following advantages:① Effective against frequency selective fading; ②Compared with domain equalization, system complexity is low, structure is simple, and peak-to-average ratio is small, which is reduced. distortion. The design of an SC-FDE structural system realized by this topic is introduced below.

4. Implementation of SC-FDE system model

In the SC-FDE system model, the receiver includes an analog-digital conversion module, a mixing filter module, a channel estimation module, a channel equalization module, and the like. In order to further reduce the bit error rate, this paper adds a channel coding and decoding module to the SC-FDE system model. The figure below is a block diagram of the SC-FDE system model.

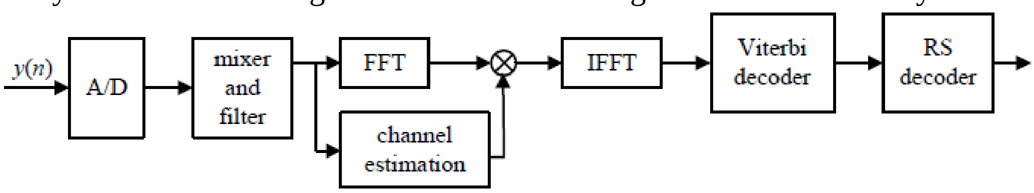

Fig.2 The SC-FDE System Model

The frame structure based on Unique Word (UW) is a data frame structure often used in a single-carrier frequency domain equalization system, and can perform frame synchronization and channel estimation work. At the beginning of each frame, the system uses a 2-segment pseudo-superimposed sequence (Zadoff-Chu) as a cyclic prefix to implement functions such as frame synchronization, channel estimation, and noise estimation. The pseudo-superimposed sequence has stable amplitude, good periodic autocorrelation and cross-correlation properties, and satisfies the fft transform retention characteristics. The pseudo-superimposed sequence performance is superior in various channel environments.

This design uses the unique word (UniW Word, UW) to complete the frame synchronization, combined with the frame header and the local pseudo-superimposed sequence and the pseudo-superimposed sequence to perform correlation operations. Due to the autocorrelation property, a pair of main peaks and several pairs of sub-peaks are obtained. (This is the effect of multipath effects). The function of frame synchronization can be realized according to the position of the peak.

Frame synchronization is done using a finite state machine design. The state machine implementation uses a three-state synchronization mechanism based on the search state-synchronous state-protected state, as shown in Figure 3.

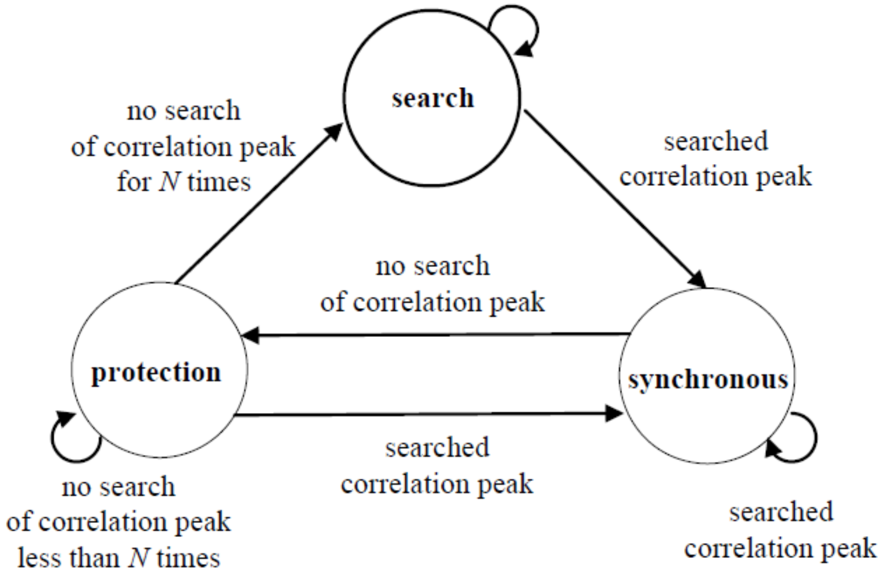

Fig.3 Three-state Synchronization Mechanism

The block diagram of the implementation of synchronization and frequency offset estimation is shown in Figure 4.

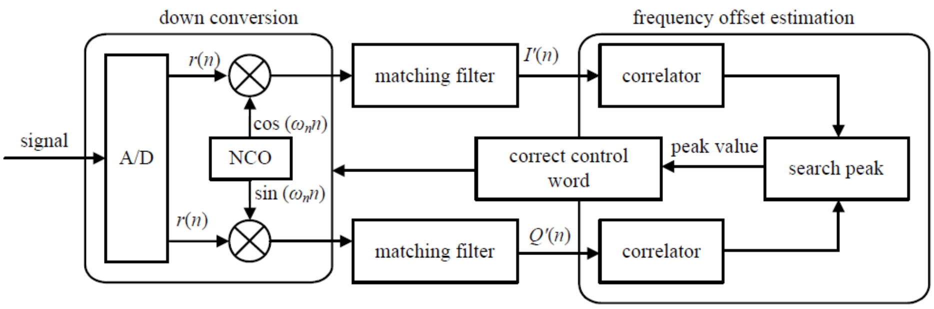

Fig. 4 The Implementation of Synchronization and Frequency Offset Estimation

5. Implementation and measurement of single-carrier frequency domain equalization system on FPGA

Single-carrier frequency domain equalization system completes design verification, debugging and actual testing on XILINX's xc4vlx160. In order to increase the transmission rate, the system adopts QPSK in the modulation mode, and configures transmit waveform parameters by matlab in transmitter. The carrier frequency and symbol rate are 137.5 MHz and 27.5 Mbps. The hardware platform observes receiver performance through oscilloscope and complete system verification and testing.

The more complex part of the system is frequency domain channel estimation and equalization. The channel estimation and equalization operations involve Fourier transform and inverse transform, divider and multiplier implementation in FPGA, and temporary storage of information using RAM. XILINX's IP core can implement most of the mathematical operations in the algorithm. The following figure shows the hardware block diagram of the system:

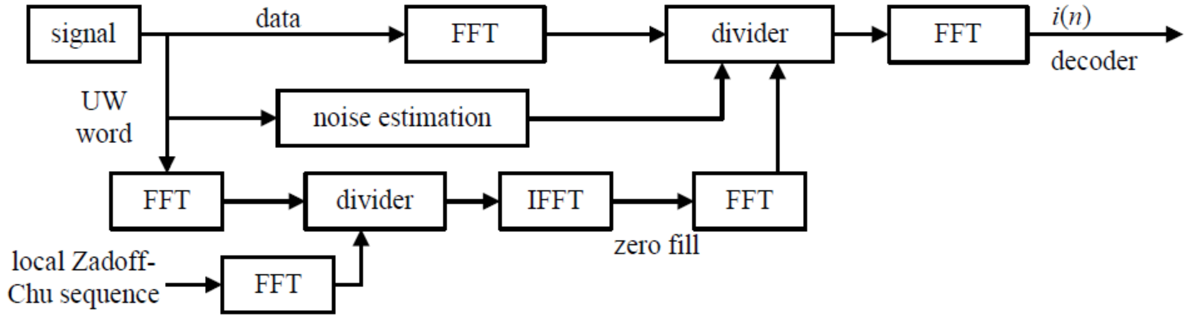

Fig.5 Frequency Domain Channel Estimation and Equalization

In the case of channel equalization, it is necessary to perform 2048 point FFT and IFFT on the received data, which causes great overhead in hardware and time, and it is difficult to satisfy the real-time processing of the system. This topic uses the ping-pong operation structure to improve the processing speed of the system, and configures the FFT core as the base 4 burst mode. Although it increases hardware overhead, it can meet real-time performance. In addition, there are also large hardware overheads for the divider. To save resources, this topic uses a look-up table instead of a divider.

The system completes the test verification on the hardware platform, and uses Matlab to write the configuration file to complete the parameter configuration of the transmitted waveform, then uses the Agilent E4438C signal source to transmit the signal. Finally, design the BER statistics module to calculate the system performance at the receiving end.

In the test environment used by this system, the main path and multipath of the channel are both one, and the multipath energy is –3 dB. When testing that there is no multipath and multipath delay of 10-50 symbols, the error rate of bit error rate received by the receiving end is shown in Table 1, Table 2, and Table 3.

Table1 Error rate statistics after equalization

R_{SN}/dB	BER					
	delay 0	delay of 10 symbols	delay of 20 symbols	delay of 30 symbols	delay of 40 symbols	delay of 50 symbols
6.5	0.003 03	0.028 27	0.028 61	0.026 16	0.033 82	0.041 18
7.0	0.001 74	0.023 27	0.022 31	0.022 05	0.027 81	0.036 01
8.0	0.000 52	0.013 63	0.013 29	0.012 82	0.018 60	0.026 36
9.0	0.000 13	0.006 93	0.007 15	0.006 95	0.012 79	0.019 15
10.0	0.000 032 75	0.003 43	0.003 48	0.003 46	0.008 25	0.014 31

Table2 Error rate statistics after Viterbi decoding

R_{SN}/dB	BER					
	delay 0	delay of 10 symbols	delay of 20 symbols	delay of 30 symbols	delay of 40 symbols	delay of 50 symbols
6.5	0	0.000 857	0.000 353	0.000 187	0.001 032	0.001 724
7.0	0	0.000 228	0.000 104	0.000 053 26	0.000 364	0.000 650
8.0	0	0.000 034 71	0.000 022 51	0.000 012 68	0.000 062 24	0.000 137
9.0	0	0.000 001 114	0.000 000 484 3	0.000 002 711	0.000 031 86	0.000 047 71
10.0	0	0.000 000 001 307	0.000 000 174 4	0.000 000 231 2	0.000 000 404 8	0.000 001 279

Table 3 Error rate statistics after RS decoding

R_{SN}/dB	BER					
	delay 0	delay of 10 symbols	delay of 20 symbols	delay of 30 symbols	delay of 40 symbols	delay of 50 symbols
6.5	0	0.000 018 79	0.000 000 488 7	0.000 000 809 4	0.000 104	0.000 112
7.0	0	0.000 000 765 4	0.000 000 008 968	0.000 000 012 61	0.000 002 288	0.000 022 52
8.0	0	0	0	0	0.000 001 283	0.000 000 014 29
9.0	0	0	0	0	0	0
10.0	0	0	0	0	0	0

As the signal-to-noise ratio decreases, the bit error rate will change greatly after equalization. When the signal-to-noise ratio drops to 6.5 dB, the bit error rate reaches 10-2. Compared with Table 1 and Table 2, the overall trend remains. In the case of Viterbi decoding under substantially identical conditions, the bit error rate drops to 10-4, except for the case of delay of 40 and 50 symbols at 6.5 dB, which indicates that Viterbi decoding effectively corrects the system after equalization. mistake.

6. Conclusion

Aiming at the deterioration of channel transmission characteristics caused by multipath effect in communication, this paper designs broadband single-carrier frequency domain equalization system and implements the system on xc4vlx160 model FPGA platform, which test the carrier frequency and symbol rate are 137.5 MHz and 27.5 Mbps respectively. And make statistics and comparison of the BER performance after equalization. The test results show that by adopting single-carrier frequency domain equalization technology in digital communication, the influence of multipath effect can be well eliminated, the system error rate can be reduced, and communication can be stably and efficiently transmitted.

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